REMARKS

I. Introduction

Applicant notes with appreciation the indication of allowable subject matter being recited by claims 2 and 3.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claim 1 Under 35 U.S.C. § 103(a)

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ueno et al. (U.S. 5,286,927) in view of Jang et al. (U.S. 5,702,977).

With regard to the present invention, claim 1, which is the sole pending independent claim, recites in part a third step for etching the insulating film using an etching mask having a lattice window pattern in such a manner that lattice openings corresponding to the lattice window pattern are formed in the first region. The lattice windows are used in the active region having the relatively large area when the insulating film on the surface of the semiconductor substrate is etched. As a result, any remaining part of the insulating film is supplemented in the active region having the relatively large area so that the decreasing rate of the insulating film thickness during the polishing process by the CMP method is effectively equalized across the entire surface.

In contrast to the claimed invention, Jang, et al. recites that there exists the trench for dividing the surface of the semiconductor substrate into the region having the relatively small

area. However, there is no mention in the cited references that the etching is carried out using the mask having the lattice windows on the region having the relatively large area.

Ueno recites that the etching is carried out when the groove is formed. However, there is no mention in the cited references that the etching is carried out on the region having the relatively large area isolated by the groove. Accordingly, the cited references neither disclose nor suggest that the remaining part of the insulating film is supplemented using the etching mask having the lattice window.

In the June 6, 2005 Office Action, the Examiner asserts that the third step for etching the insulating film using an etching mask (34) having a lattice window pattern (40) in such a manner that lattice openings corresponding to the lattice window pattern are formed in the first region is disclosed in column 10, lines 29-47 of the Jang et al. reference. However, it is unclear as to which passage of the cited paragraph the Examiner is referring. Column 10, lines 29-47 recites:

> Referring now to FIG. 8, there is shown a schematic cross-sectional diagram illustrating the results of further processing the thermally oxidized semiconductor substrate 30' whose schematic cross-sectional diagram is illustrated in FIG. 7. Shown in FIG. 8 is the thermally oxidized semiconductor substrate 30' as illustrated in FIG. 7, wherein the second ozone assisted thermal chemical vapor deposited (CVD) silicon oxide layer 42 is planarized through the second chemical mechanical polish (CMP) planarizing method to form the patterned planarized second ozone assisted thermal CVD silicon oxide layers 42a and 42b. The second CMP planarizing method is employed until there is reached the patterned silicon nitride layers 34a, 34b and 34c, thus simultaneously forming a series of polished patterned silicon nitride layers 34a', 34b' and 34c', along with a pair of planarized patterned conformal first ozone assisted thermal CVD silicon oxide layers 40a' and 40b'.

Thus, as can be seen in the paragraph, the prior art discloses an insulating film (42) that is polished off the substrate via CMP. While an etching mask (34) is disclosed, the Examiner's assertion that the CVD silicon oxide layers (40) correspond with or are designed in the form of a

lattice window pattern is clearly **not** disclosed in this passage or any other passage in the cited prior art. The figures to which the Examiner is referring show a trench with no indication of a lattice window pattern delineated therein. There is especially no mention of lattice openings corresponding to a lattice window pattern being formed in the first region.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA). In the instant case, the pending rejection does not "establish *prima facie* obviousness of the claimed invention" as recited in claim 1 because the proposed combination fails to disclose or suggest all of the claim limitations recited in claim 1. Therefore, for the foregoing reasons, it is respectfully submitted that the § 103 rejection based upon the proposed combination of Ueno et al. in view of Jang et al. is improper.

III. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully submitted.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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